

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Eugene H. Cloud
 Title: HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY

Docket No.: 303.663US1
 Filed: March 3, 2000
 Examiner: Than Vinh Nguyen

Serial No.: 09/518,338
 Due Date: June 13, 2002
 Group Art Unit: 2187

**COPY OF PAPERS
 ORIGINALLY FILED**

Commissioner for Patents
 Washington, D.C. 20231



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We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Amendment and Response (9 Pages).
- ☒ A Clean Version of Pending Claims (7 pgs.).

If an additional fee is required due to changes to the claims, the fee has been calculated as follows:

CLAIMS AS AMENDED						
	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Present Extra	Rate	Fee
TOTAL CLAIMS	31	-	21	10	x 18 =	\$180.00
INDEPENDENT CLAIMS	13	-	8	5	x 84 =	\$420.00
[] MULTIPLE DEPENDENT CLAIMS PRESENTED						\$0.00
TOTAL						\$600.00

Please charge the required fee of \$600.00 to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 13 day of June, 2002.

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(GENERAL)

S/N 09/518,338

PATENT

SC
#3A
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Examiner: Than Vinh Nguyen

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Title: HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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Applicant has reviewed the Office Action mailed on March 13, 2002. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect cancellation of claim 3, amendment of previously pending claims 1, 2, 4-6, 8-12, and 15-21, and addition of new claims 22-32. The specific amendments to individual claims are detailed in the following marked up set of claims.

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1. (Amended) A memory device comprising:
a volatile main memory;
a cache memory connected to the volatile main memory; and
a compression and decompression engine connected between the volatile main memory and the cache memory, wherein the volatile main memory, the cache memory, and the compression and decompression engine are located in a single chip.
2. (Amended) The memory device of claim 1 further comprising, on the single chip, an error detection and correction engine connected to the volatile main memory and the compression and decompression engine.
4. (Amended) A memory device comprising:
a [main] dynamic memory;

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01 FC:103 180.00 CH
02 FC:102 420.00 CH